

665280-7928E60

Original Image

Video Signal  
of Each Line

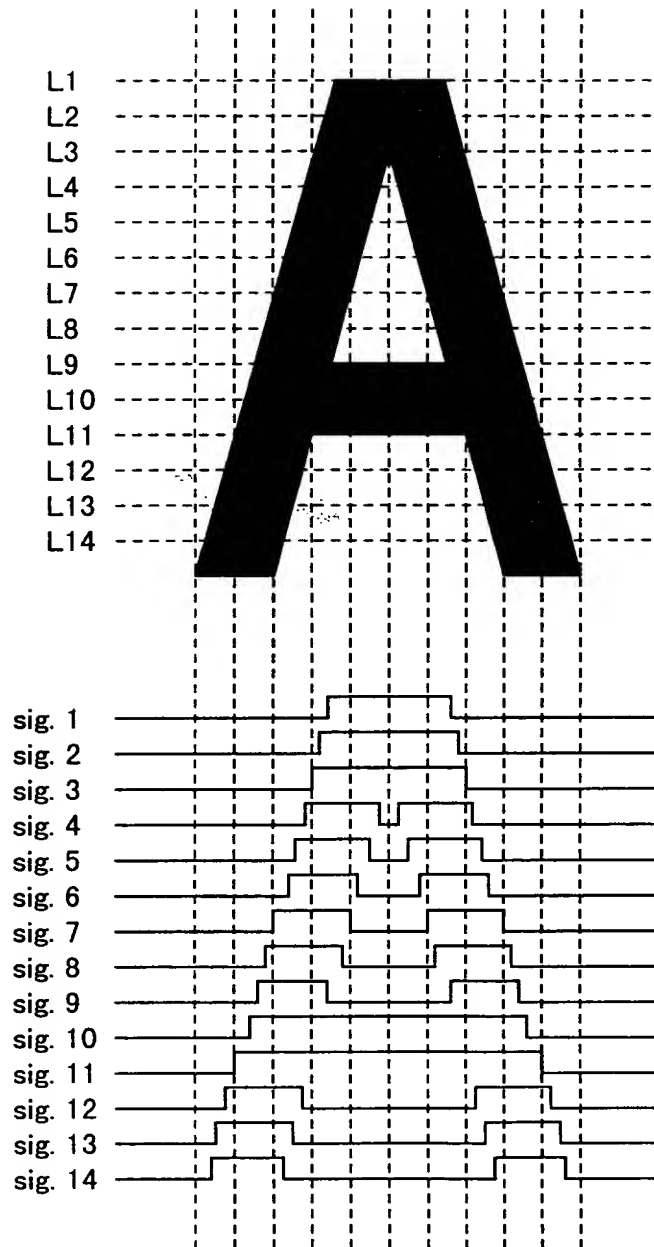


Fig. 1

09382677.082599

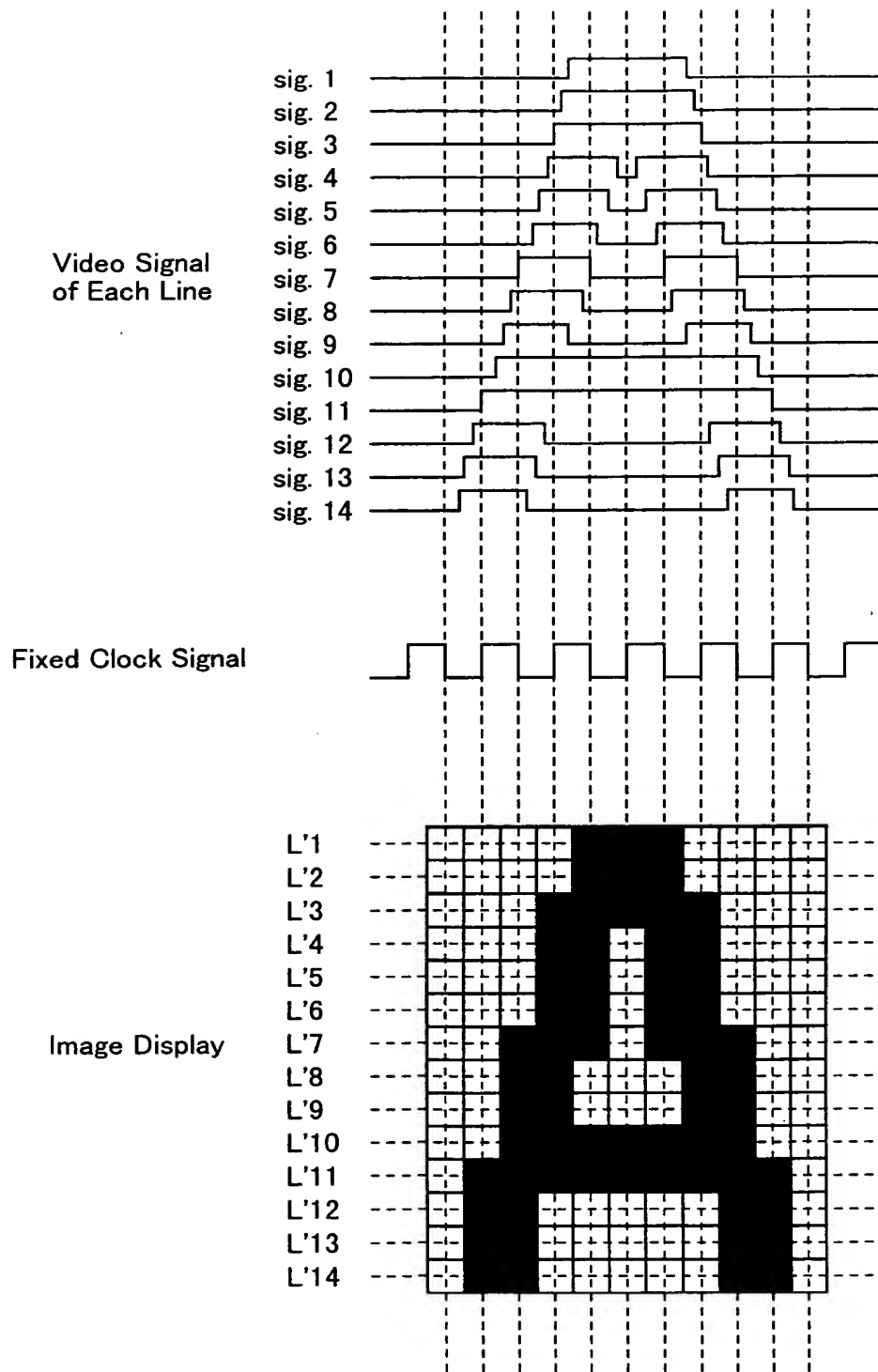
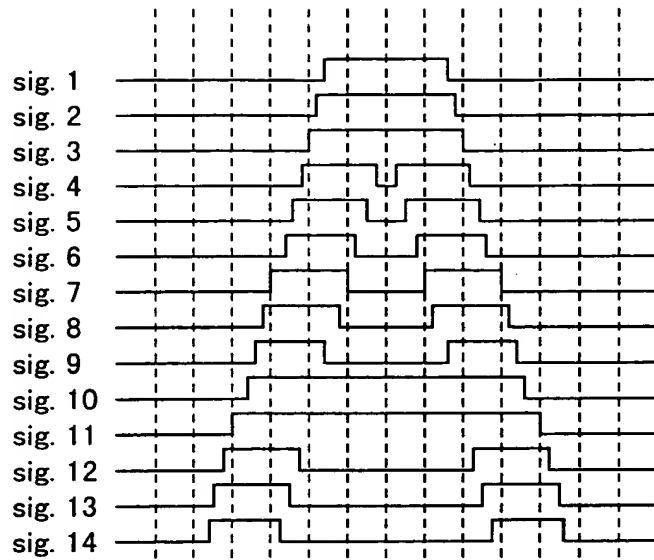


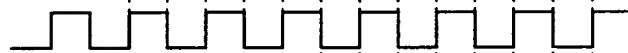
Fig. 2

09382677.082599

Video Signal  
of Each Line



Fixed Clock Signal



Modified Clock  
Signal

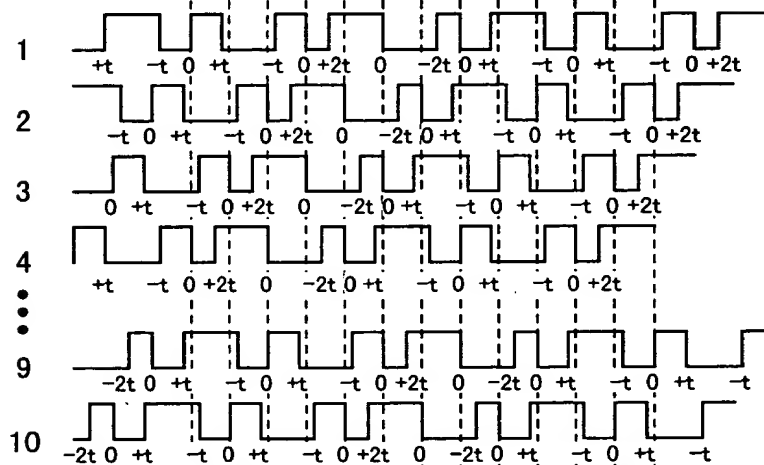


Image Display

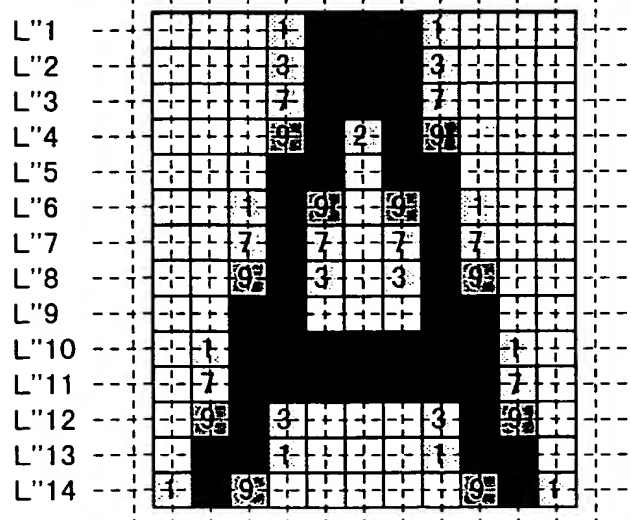


Fig. 3

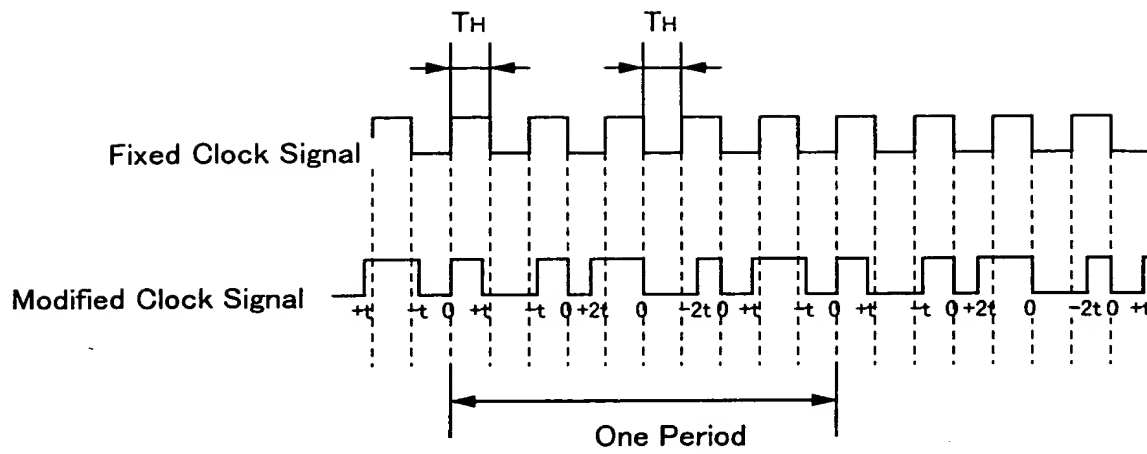


Fig. 4(A)

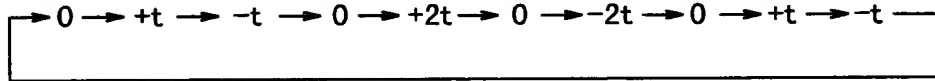


Fig. 4(B)

displacement					frequency / 10
+2t	*				1
+t	*	*			2
0	*	*	*	*	4
-t	*	*			2
-2t	*				1

Fig. 4(C)

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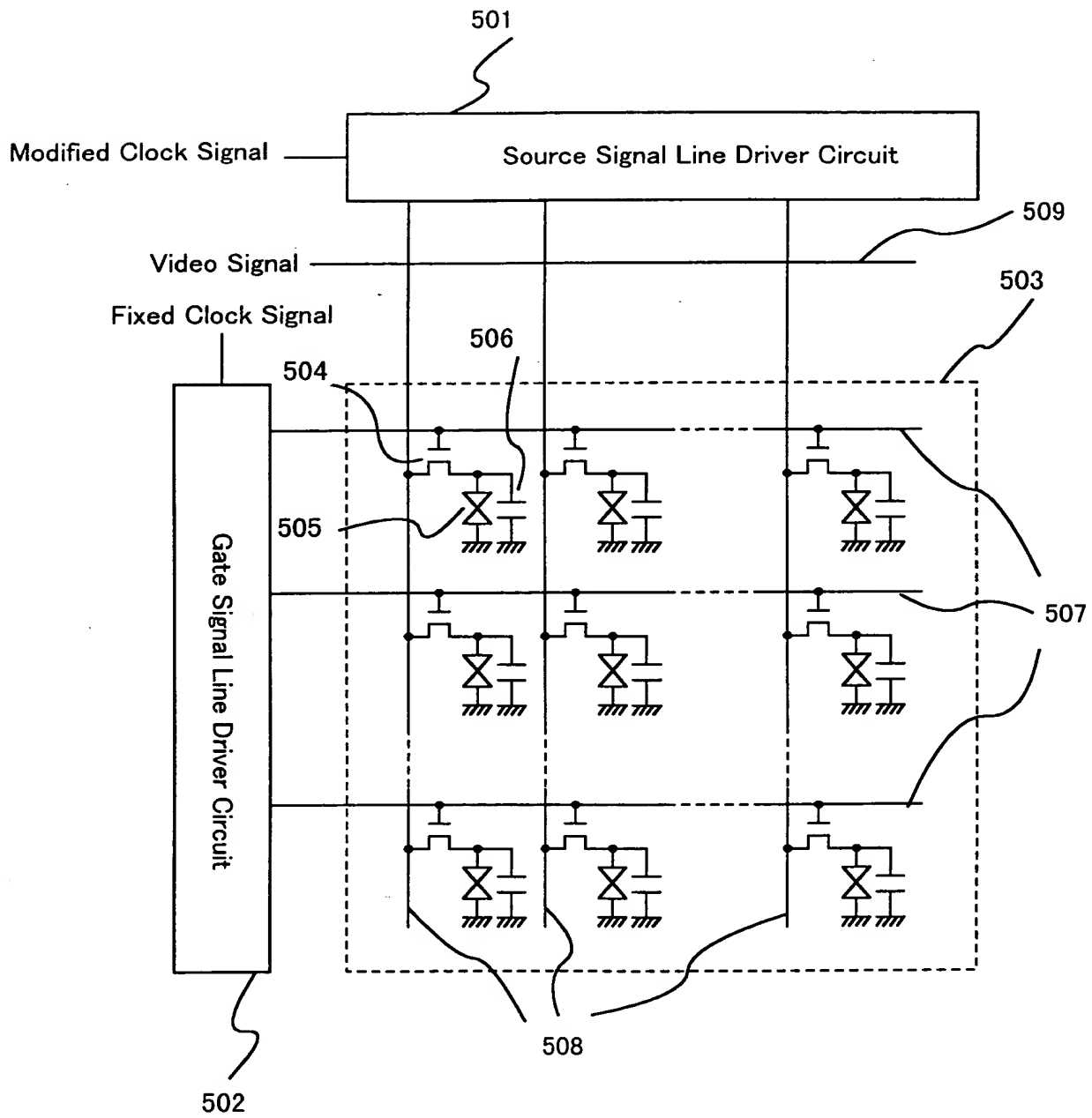


Fig. 5

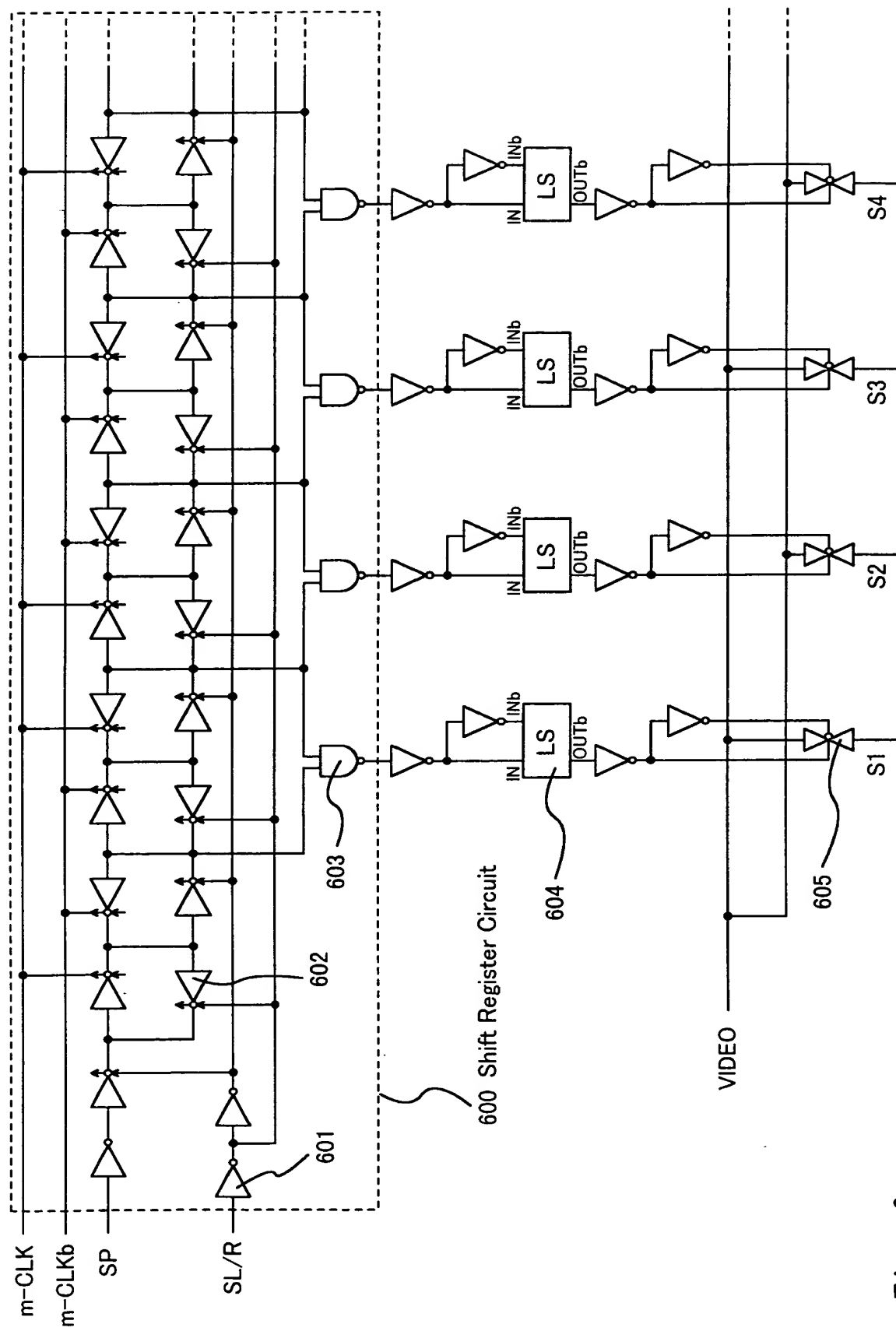


Fig. 6

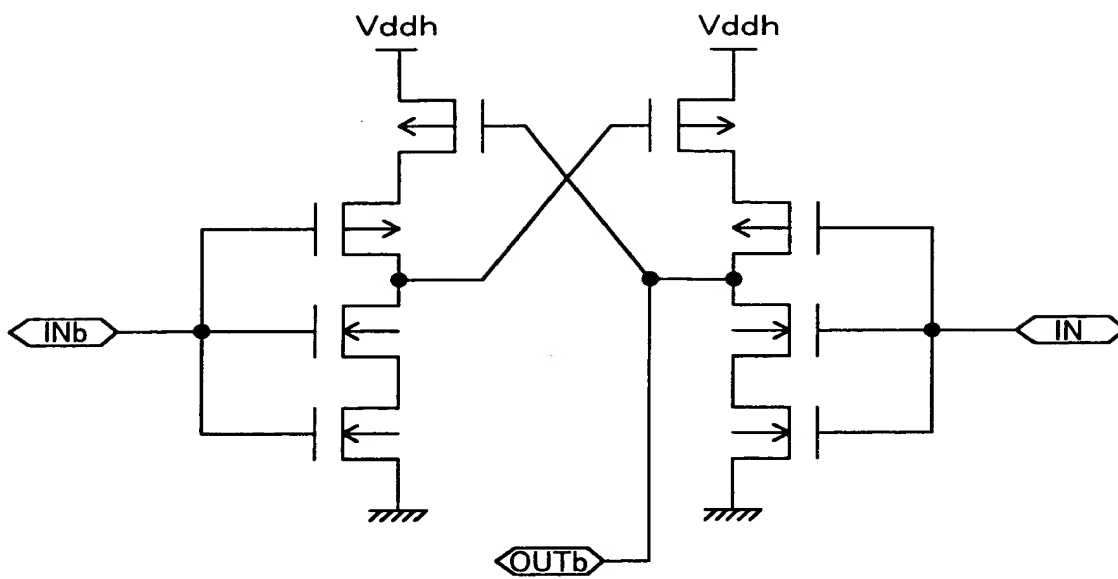


Fig. 7

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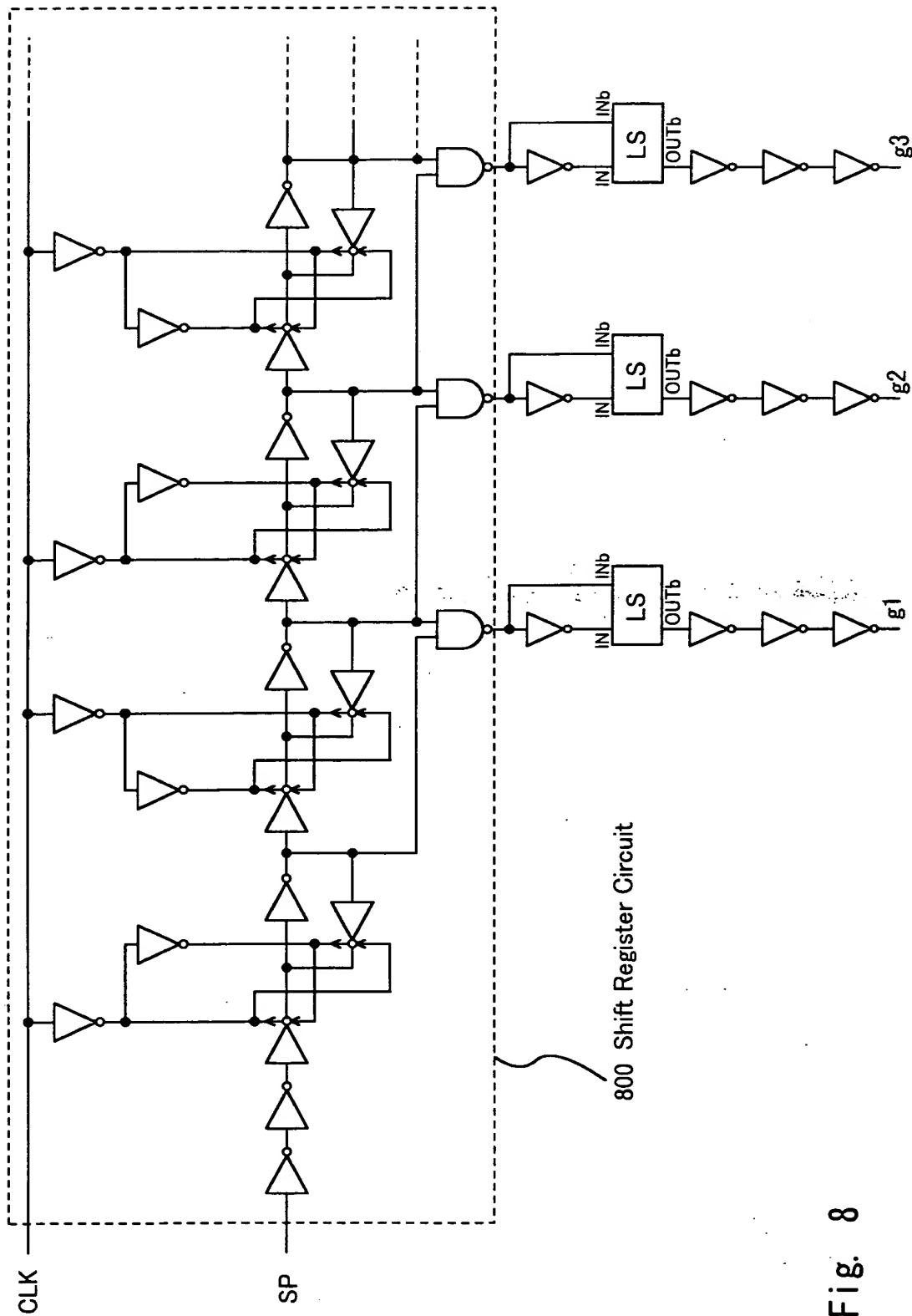
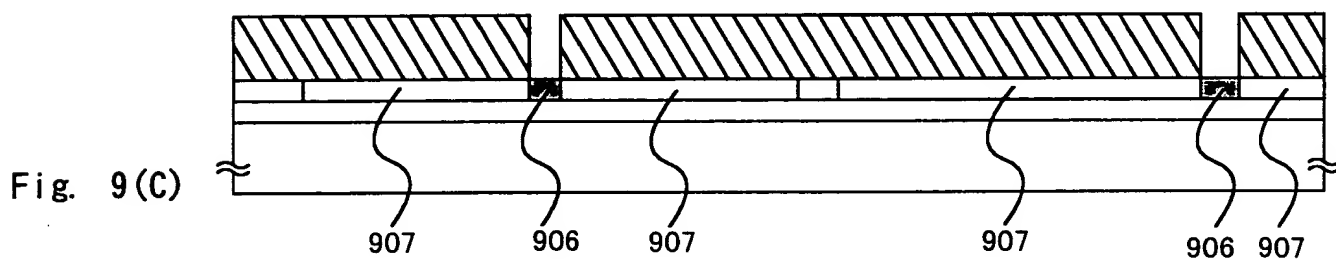
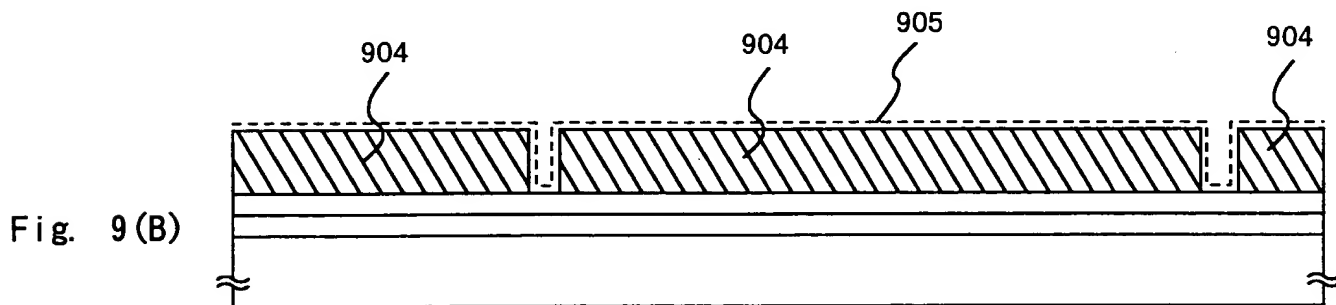
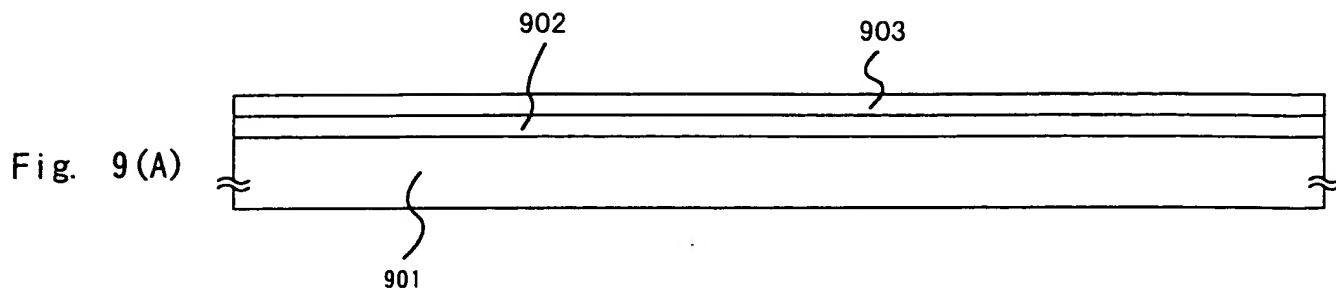


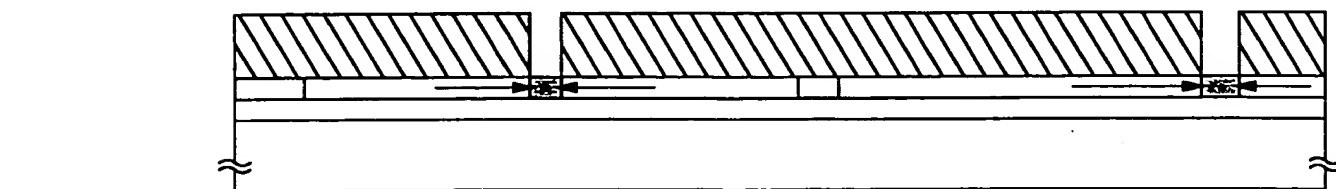
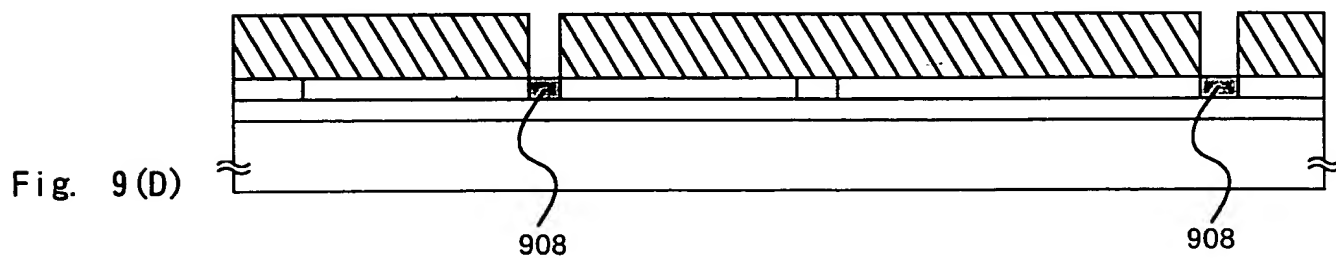
Fig. 8



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↓ ↓ ↓ ↓ ↓ ↓ P Ions Addition ↓ ↓ ↓ ↓ ↓ ↓



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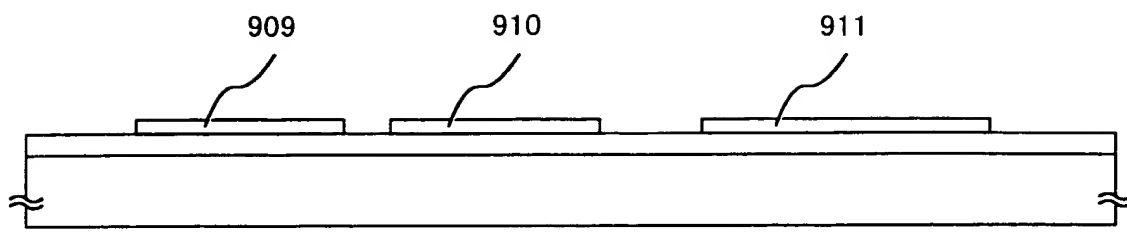


Fig. 10(A)

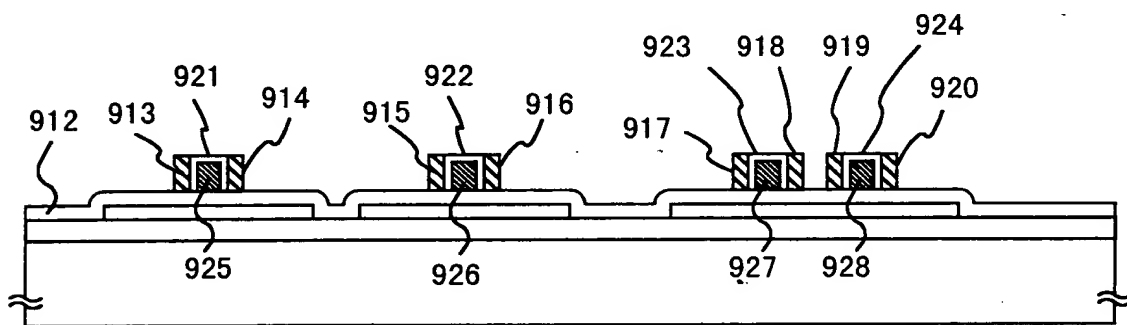


Fig. 10(B)

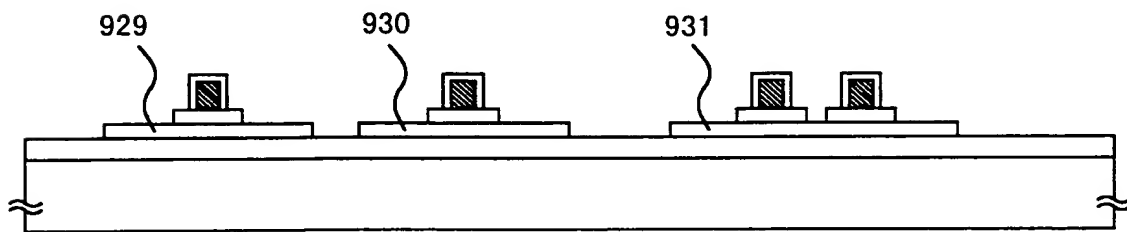


Fig. 10(C)

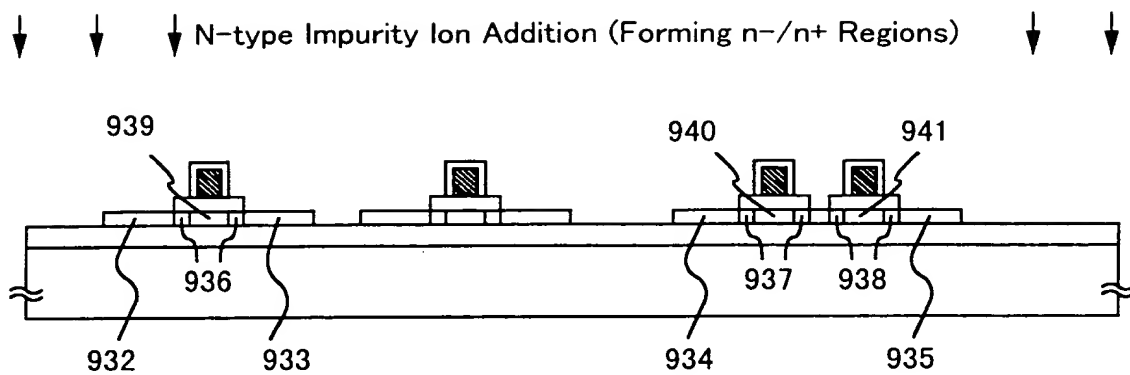


Fig. 11(A)

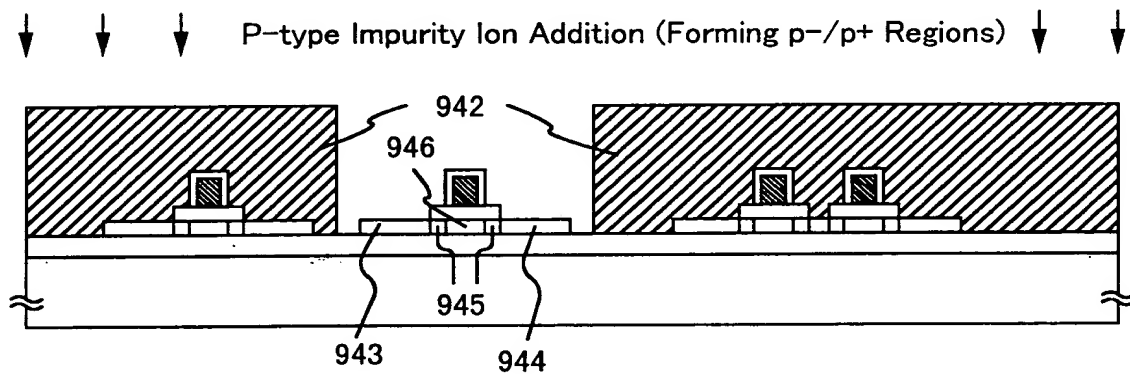


Fig. 11(B)

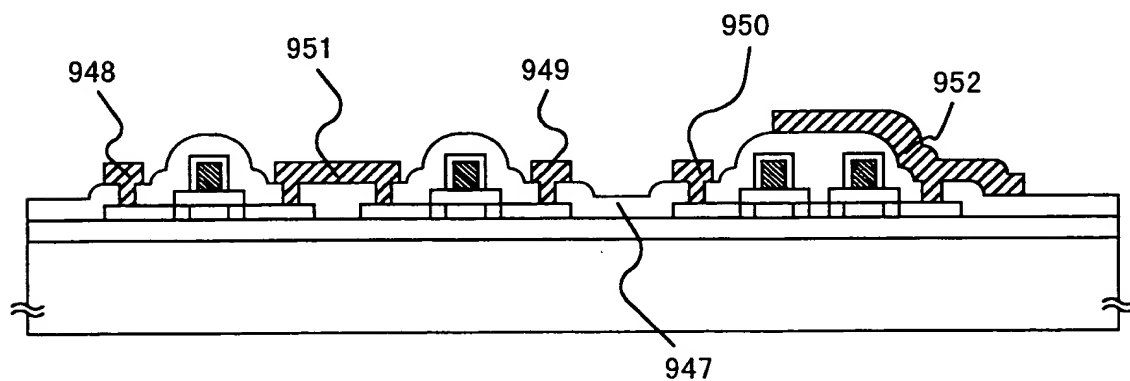


Fig. 11(C)

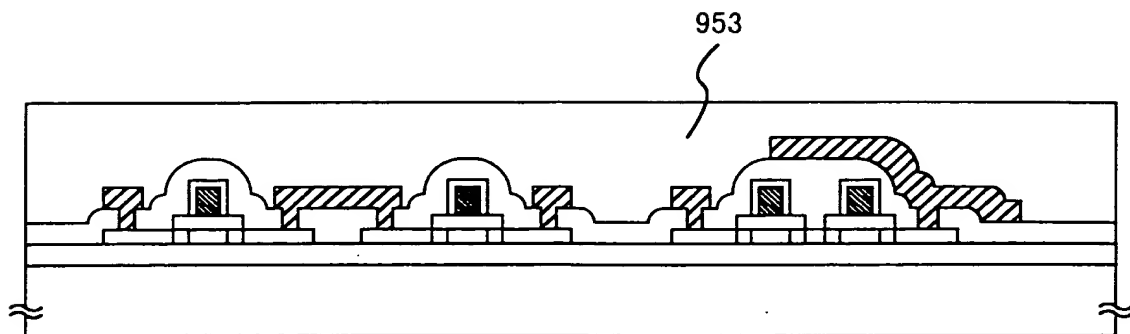


Fig. 12(A)

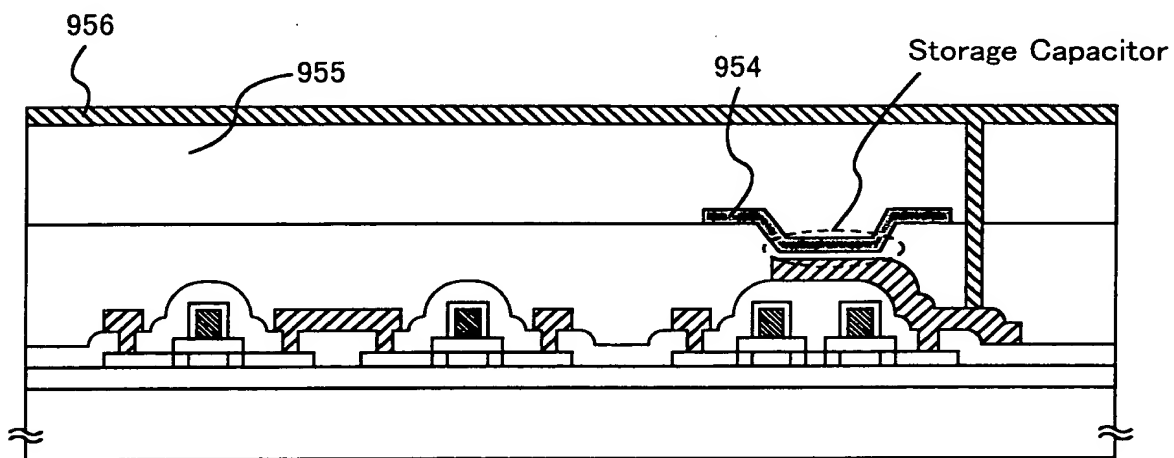


Fig. 12(B)

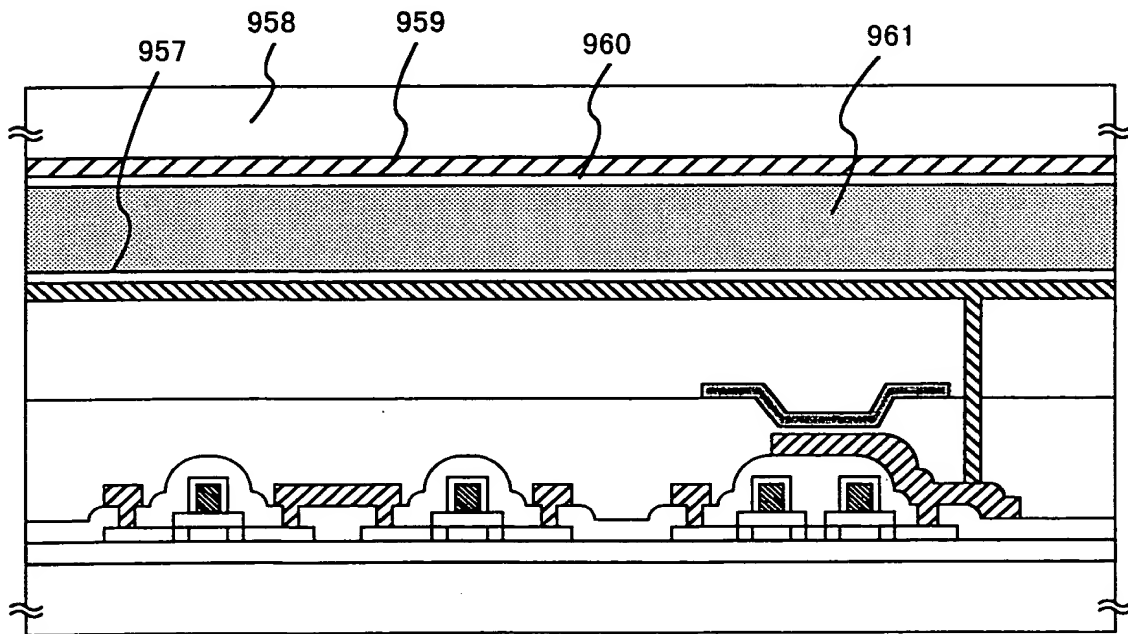


Fig. 12(C)

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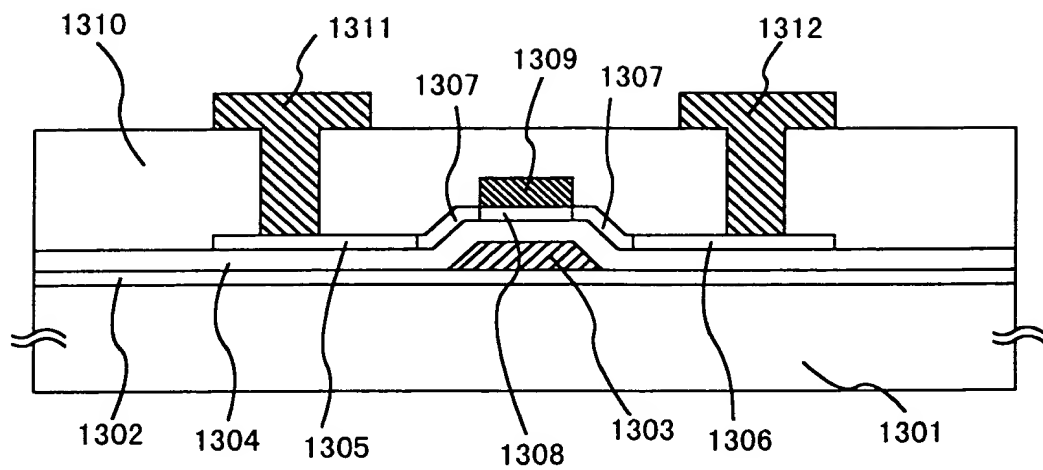


Fig. 13

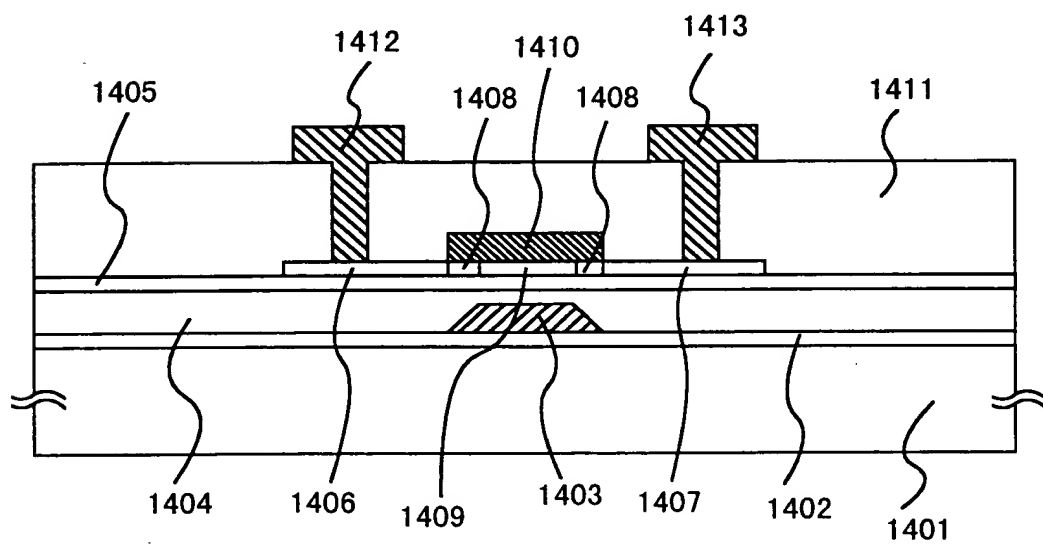


Fig. 14

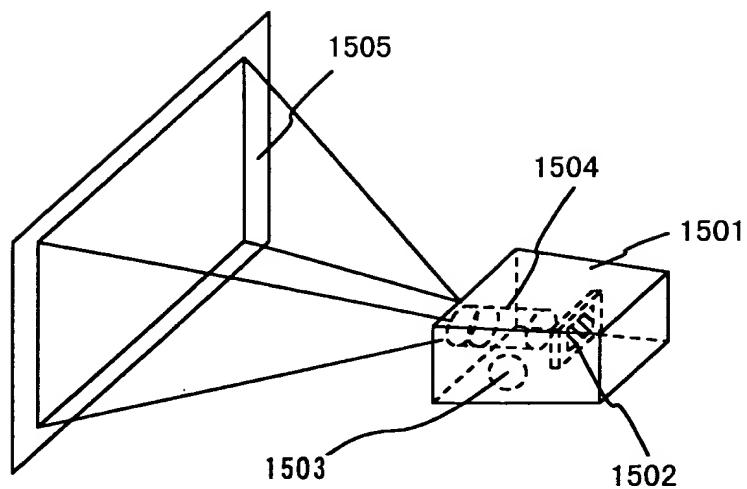


Fig. 15(A)

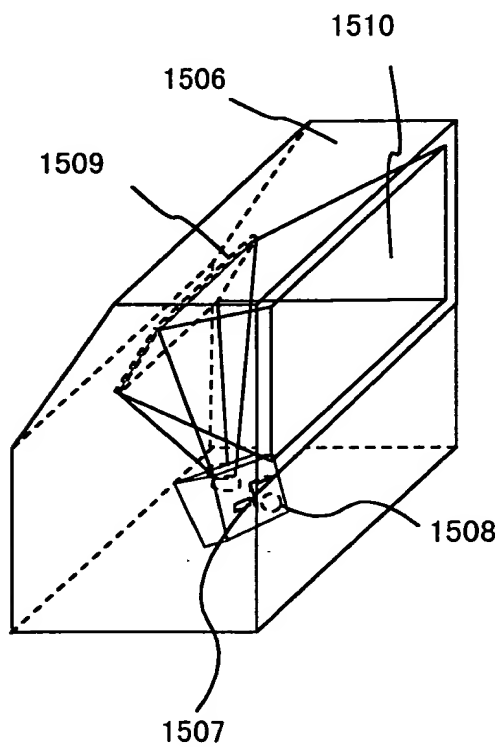


Fig. 15(B)

Fig. 16(A)

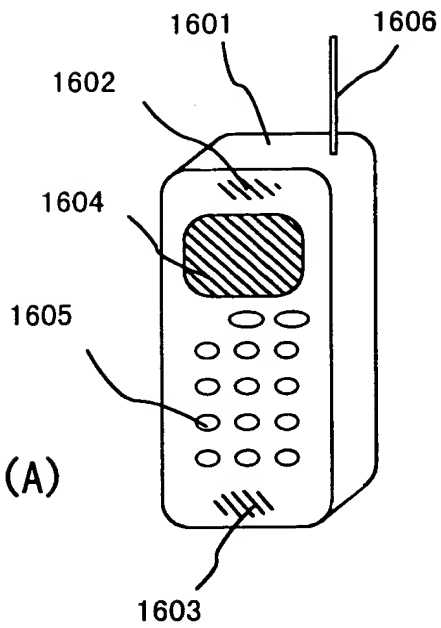


Fig. 16(B)

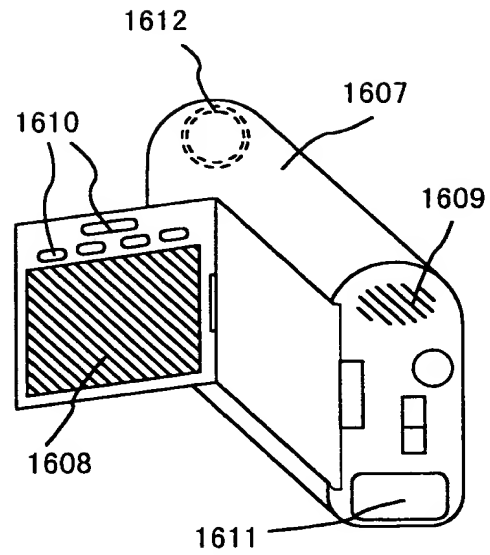


Fig. 16(C)

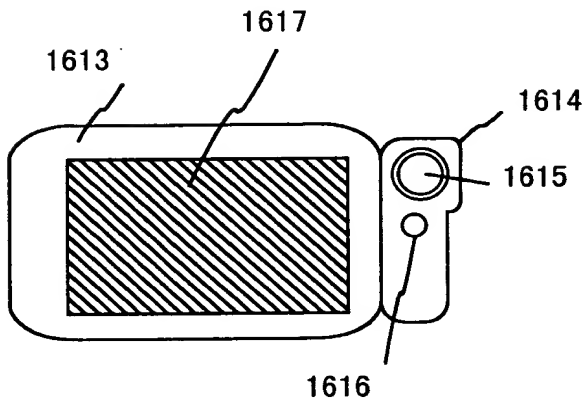


Fig. 16(D)

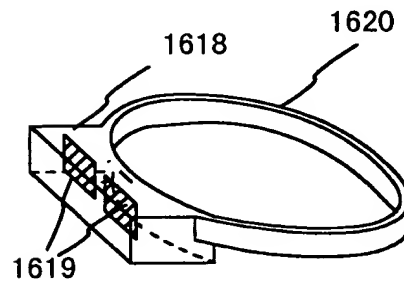
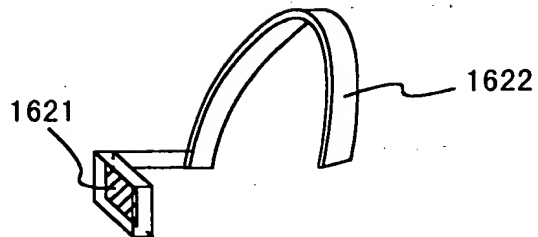


Fig. 16(E)



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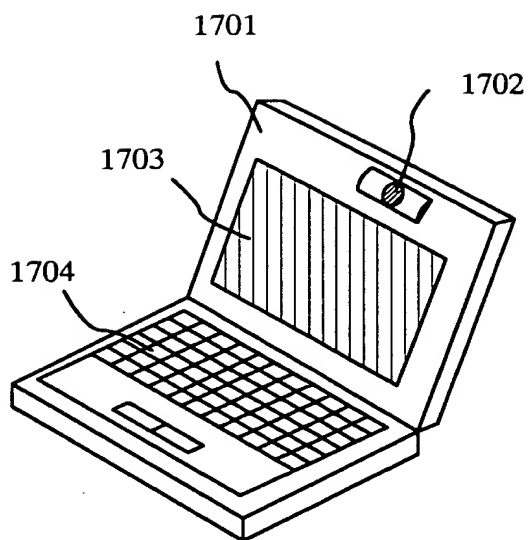


Fig. 17(A)

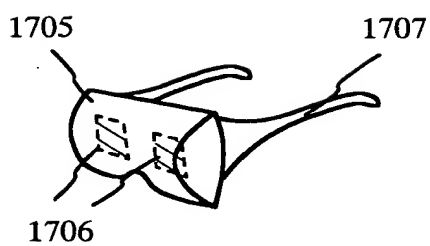


Fig. 17(B)

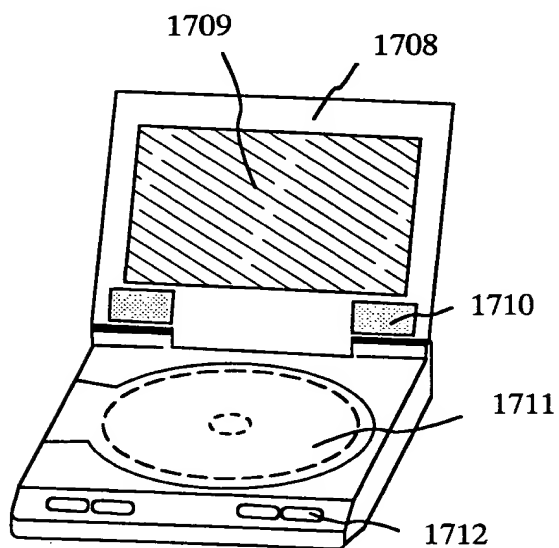


Fig. 17(C)

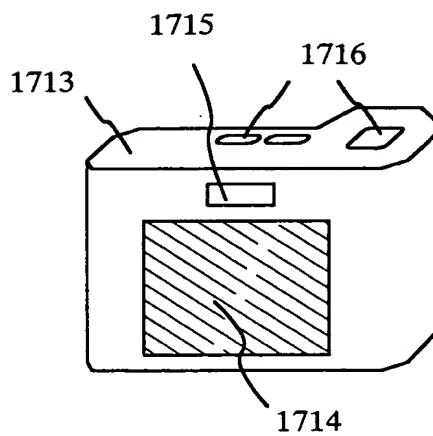


Fig. 17(D)



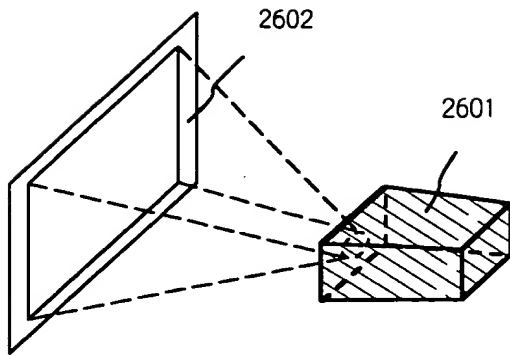


Fig. 18(A)

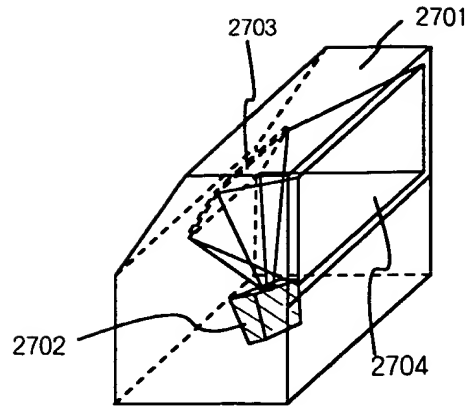


Fig. 18(B)

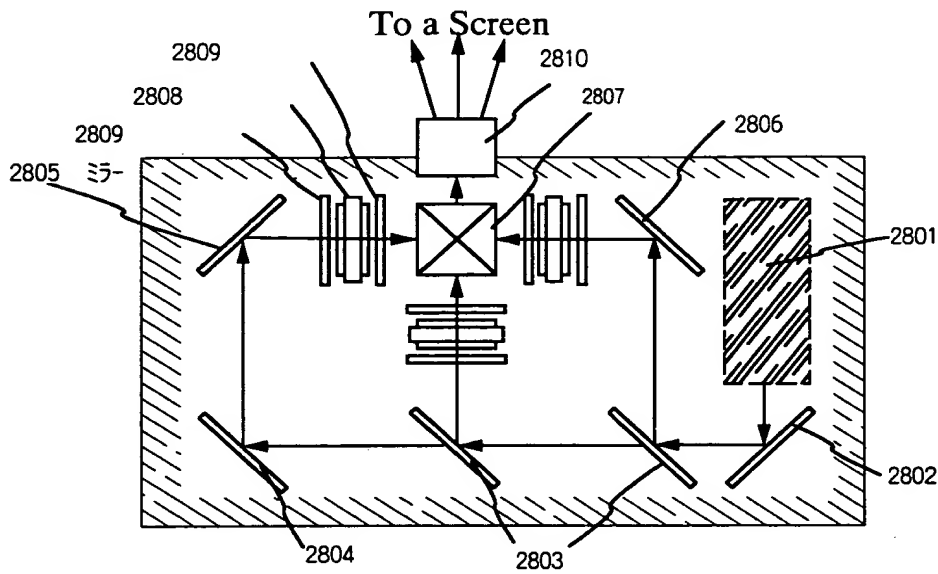


Fig. 18(C) Display Device(3 panel projector)

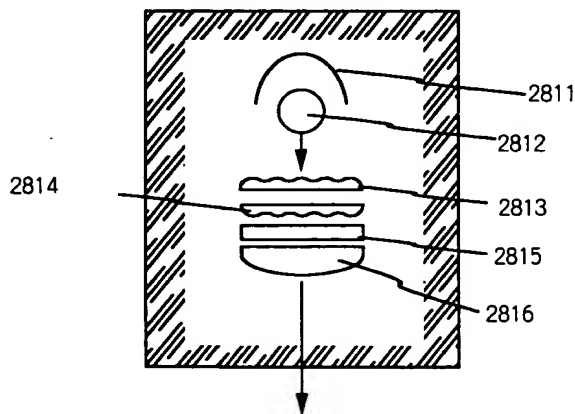


Fig. 18(D) Light Source Optical System

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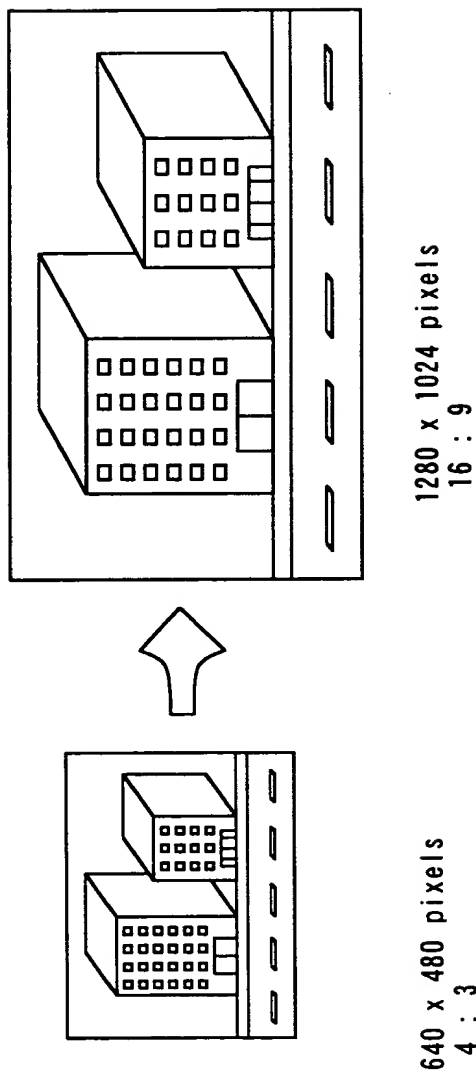


Fig. 19

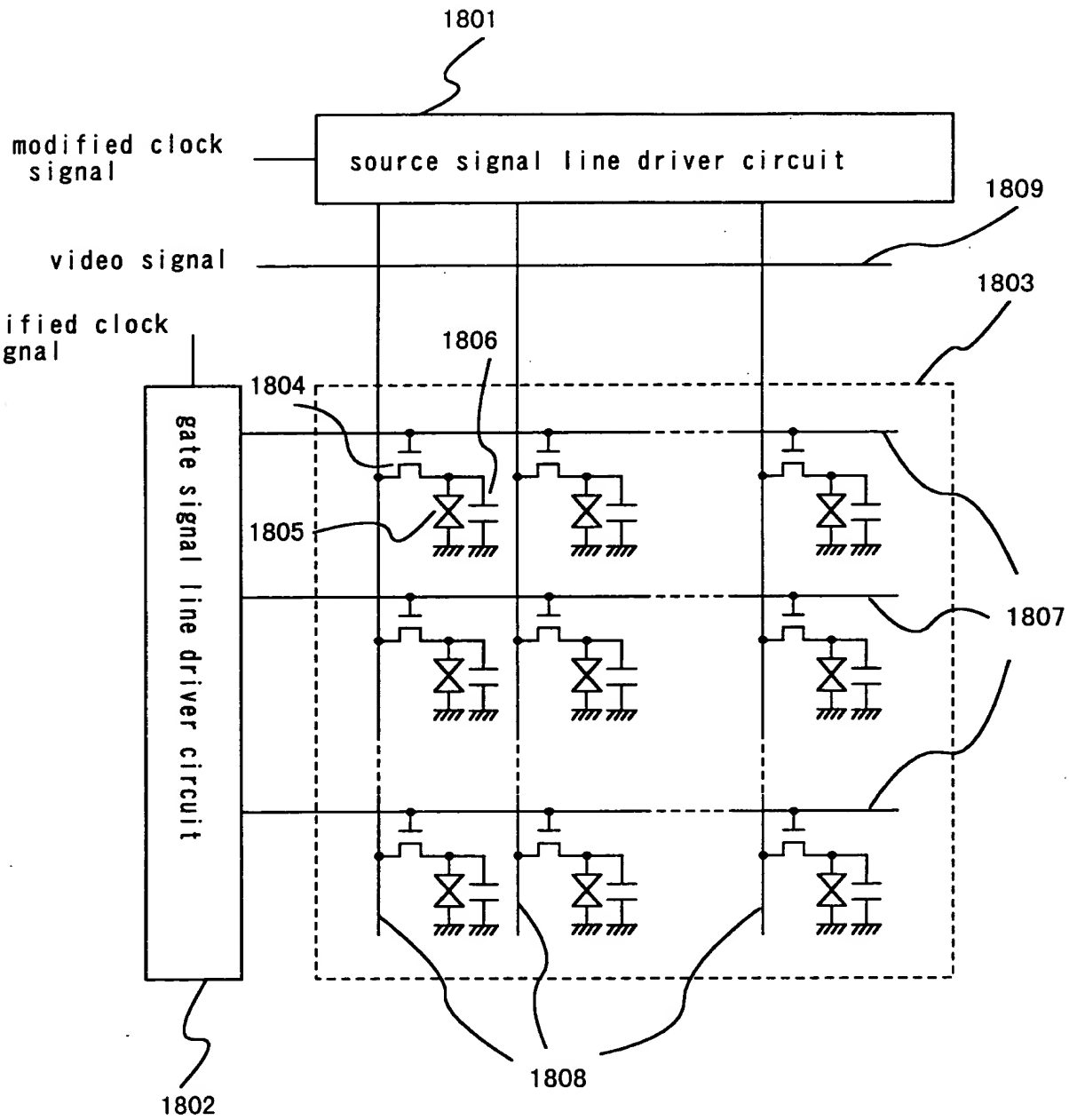
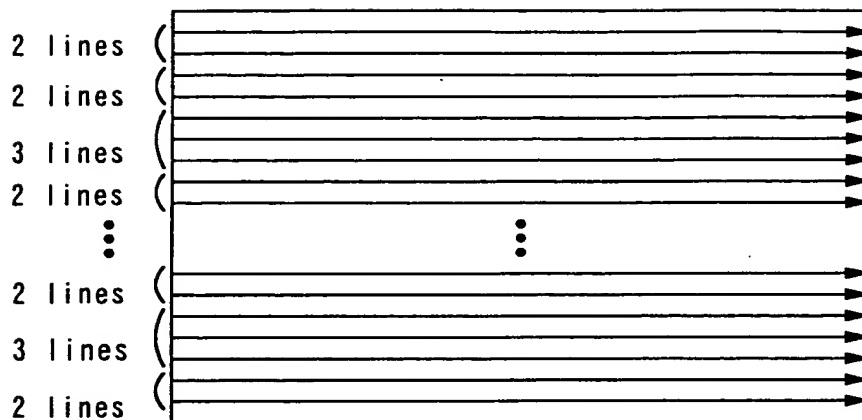


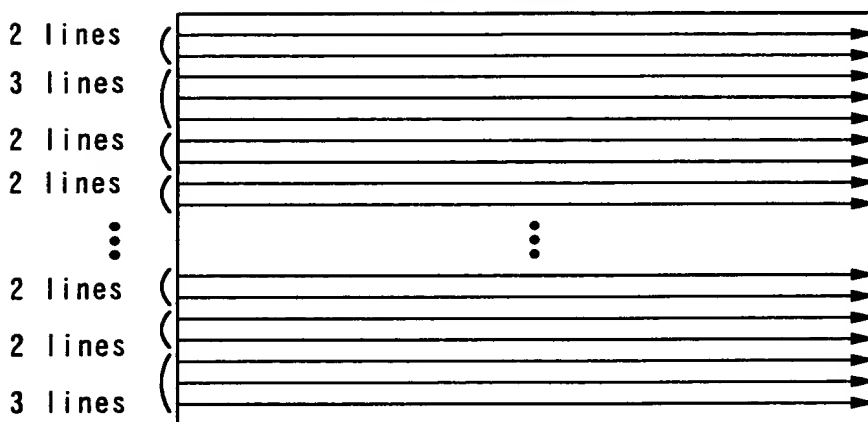
Fig. 20

Fig. 21

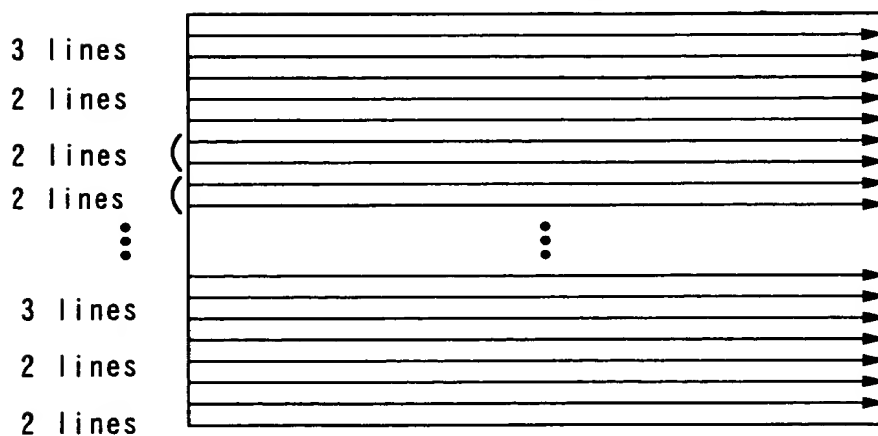
1st frame



2nd frame



n th frame



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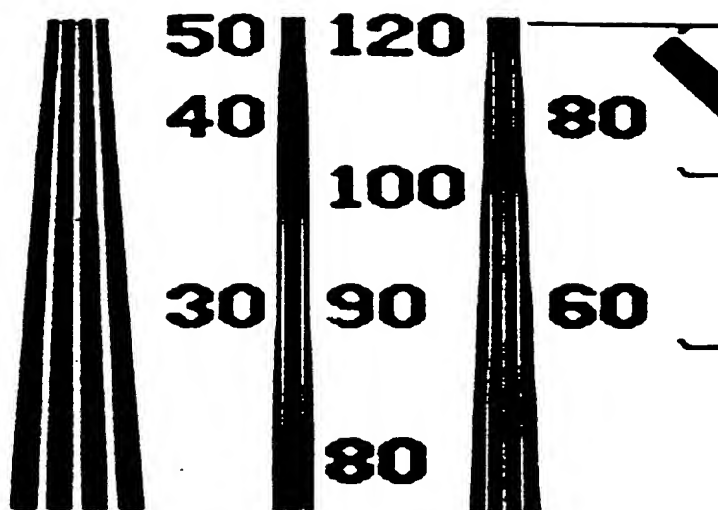


Fig. 22

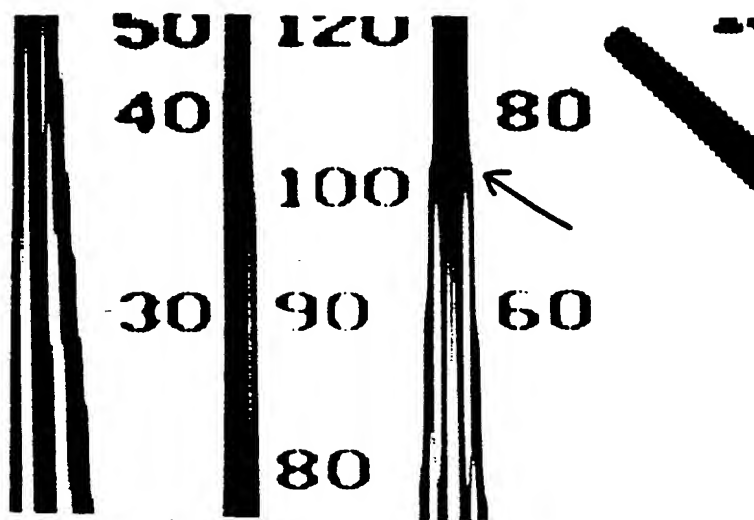


Fig. 23

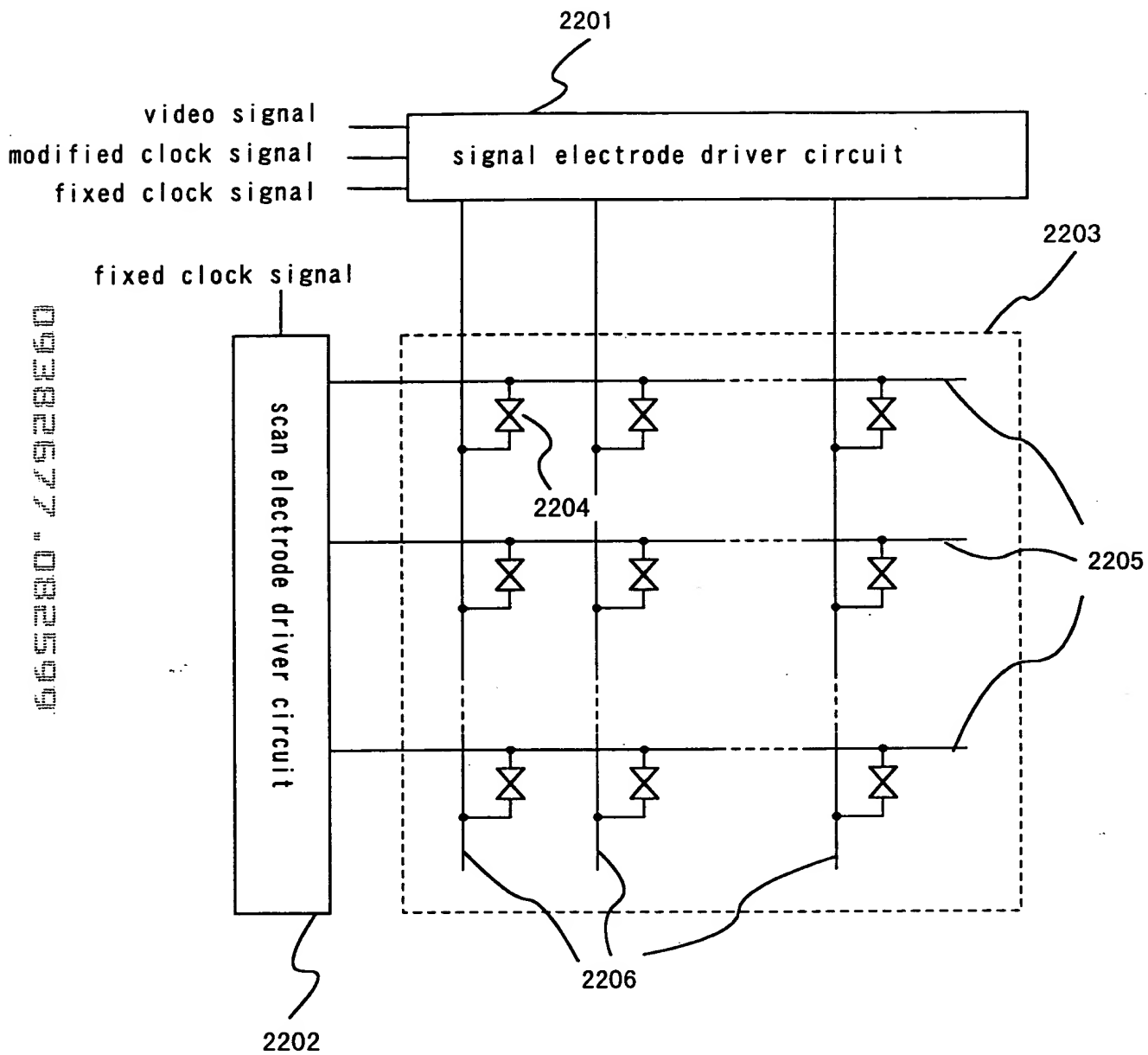
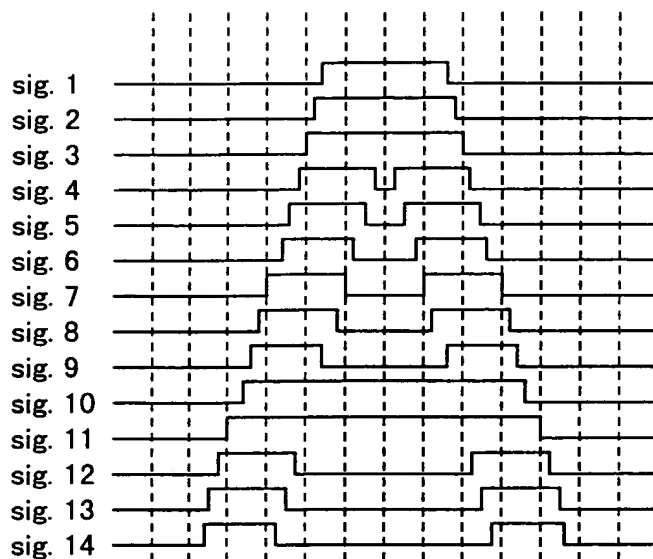


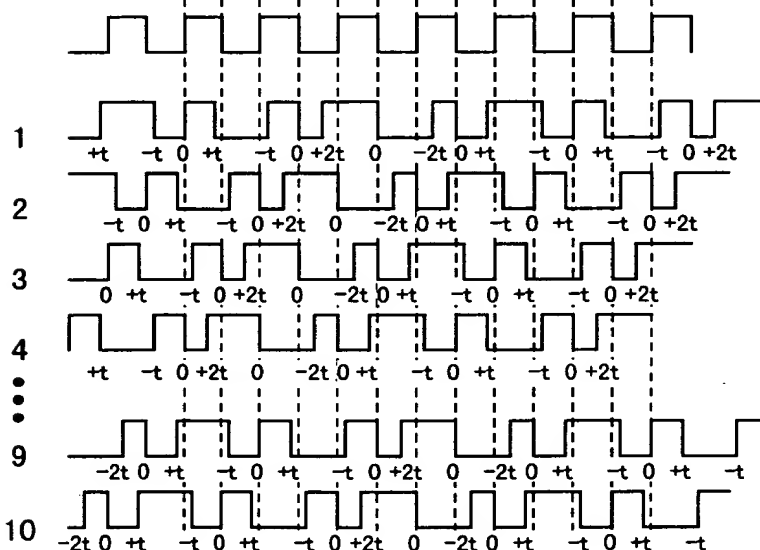
Fig. 24

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Video signals  
of each line



Fixed clock  
signal



Modified clock  
signal

Image display

L"1	--	--	--	--	1	10	10	10	1	--	--	--
L"2	--	--	--	--	3	10	10	10	3	--	--	--
L"3	--	--	--	--	7	10	10	10	7	--	--	--
L"4	--	--	--	--	9	10	2	10	9	--	--	--
L"5	--	--	--	--	10	10	--	10	10	--	--	--
L"6	--	--	--	--	1	10	9	--	9	10	1	--
L"7	--	--	--	--	7	10	7	--	7	10	7	--
L"8	--	--	--	--	9	10	3	--	3	10	9	--
L"9	--	--	--	--	10	10	--	--	10	10	--	--
L"10	--	--	--	--	1	10	10	10	10	10	1	--
L"11	--	--	--	--	7	10	10	10	10	10	7	--
L"12	--	--	--	--	9	10	3	--	--	3	10	9
L"13	--	--	--	--	10	10	1	--	--	1	10	10
L"14	--	--	--	--	1	10	9	--	--	9	10	1

Fig. 25

Fig. 26 (A)

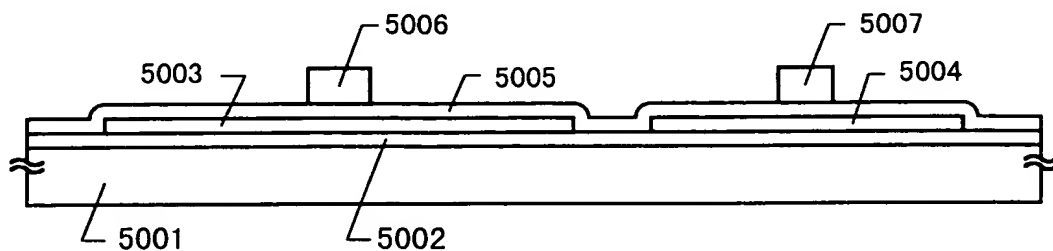


Fig. 26 (B)

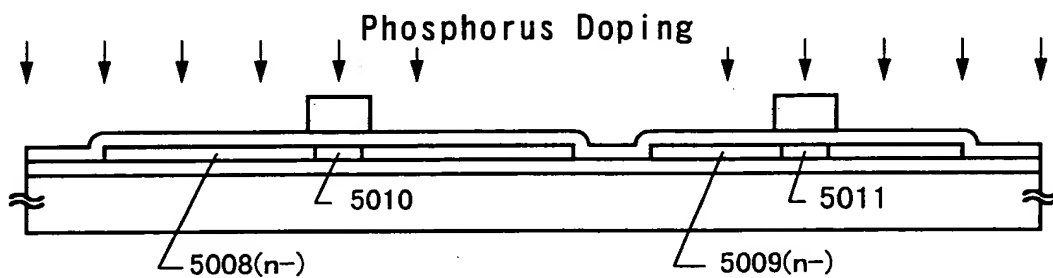


Fig. 26 (C)

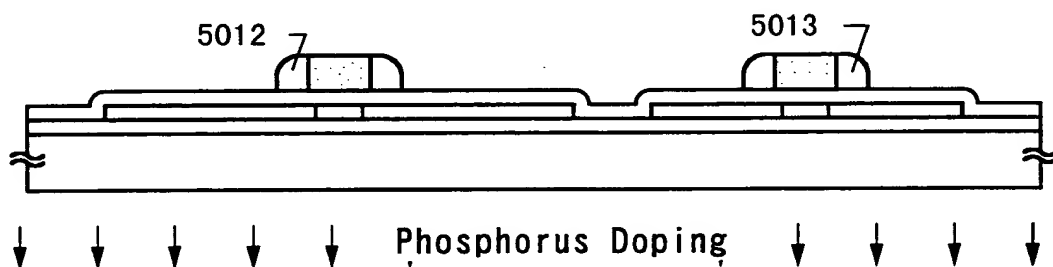


Fig. 26 (D)

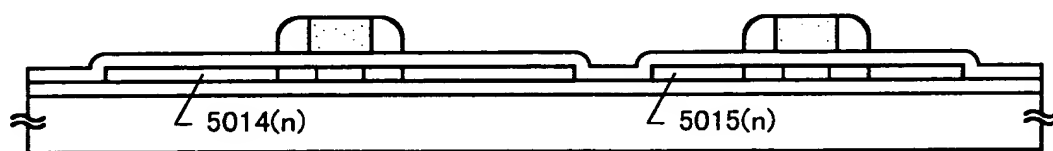
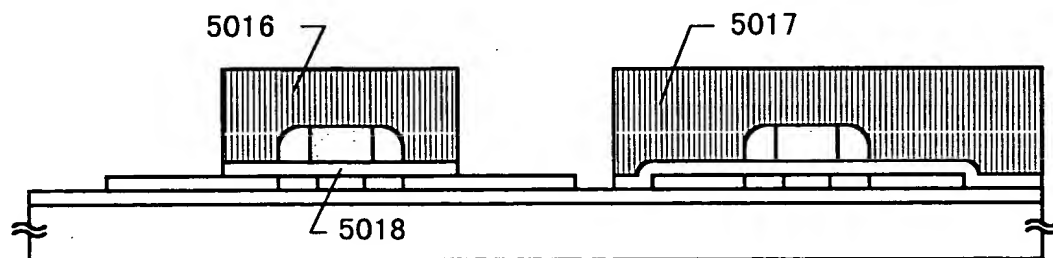


Fig. 26 (E)





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Fig. 27(A)

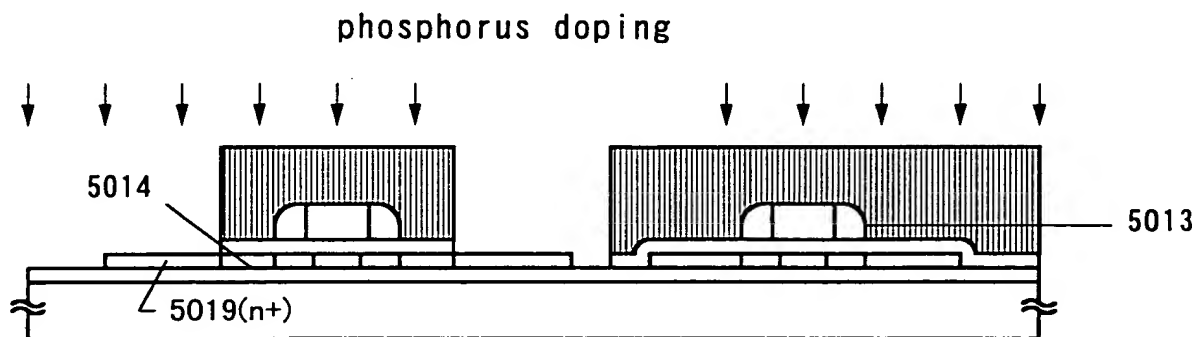


Fig. 27(B)

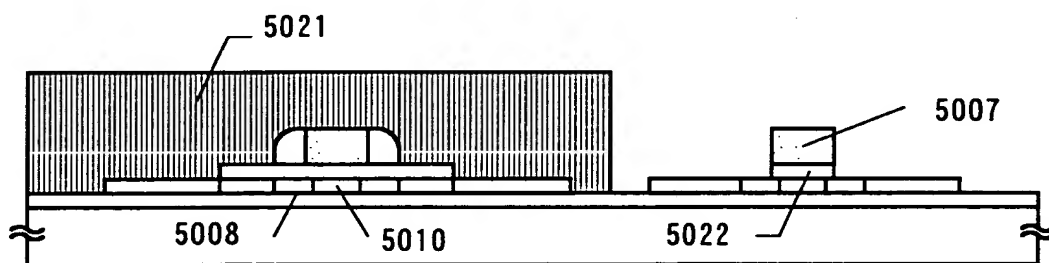


Fig. 27(C)

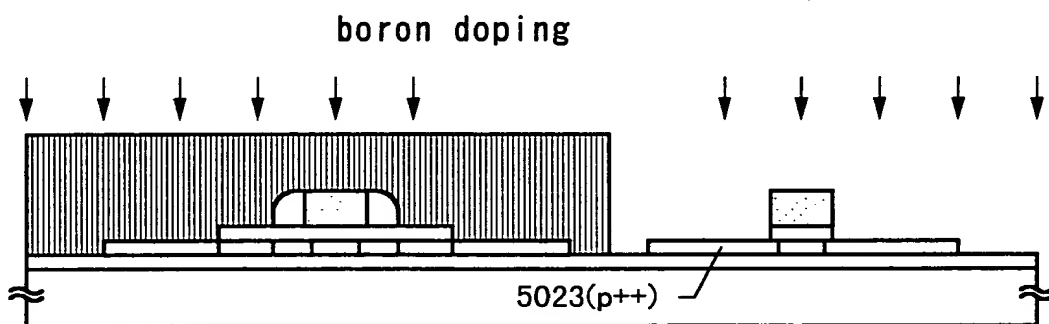
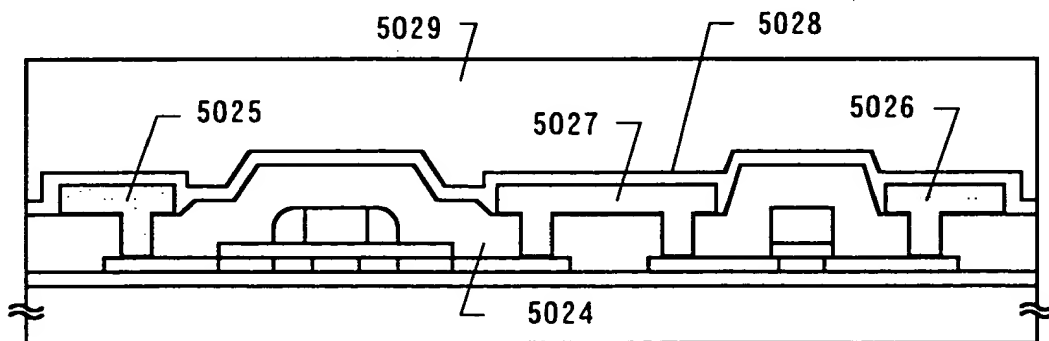


Fig. 27(D)



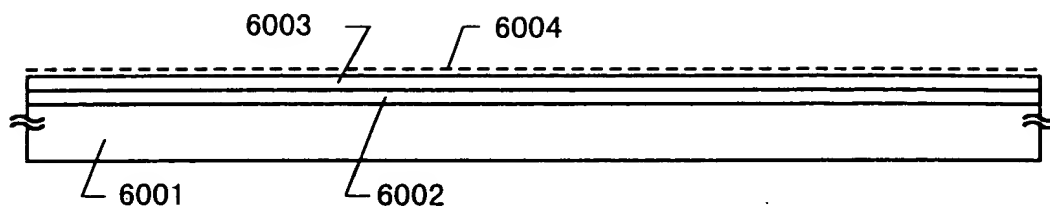


Fig. 28(A)

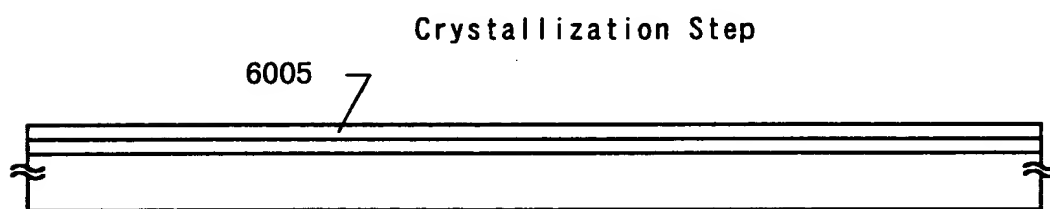
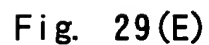
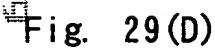
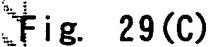
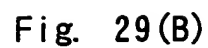
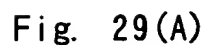


Fig. 28(B)

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n channel TFT

p channel TFT

n channel TFT

storage capacitor  
portion

## CMOS circuit

## Active matrix circuit

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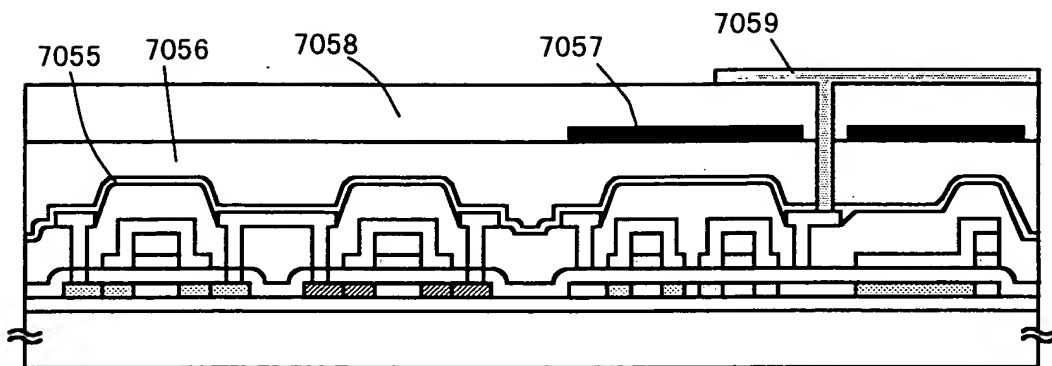


Fig. 30(A)

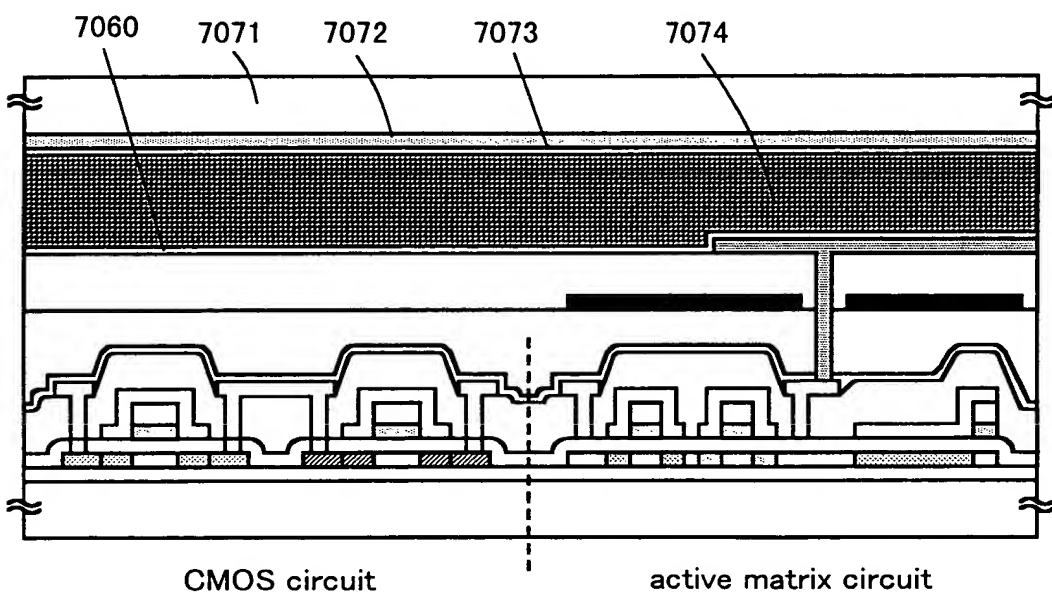


Fig. 30(B)

09382677.082599

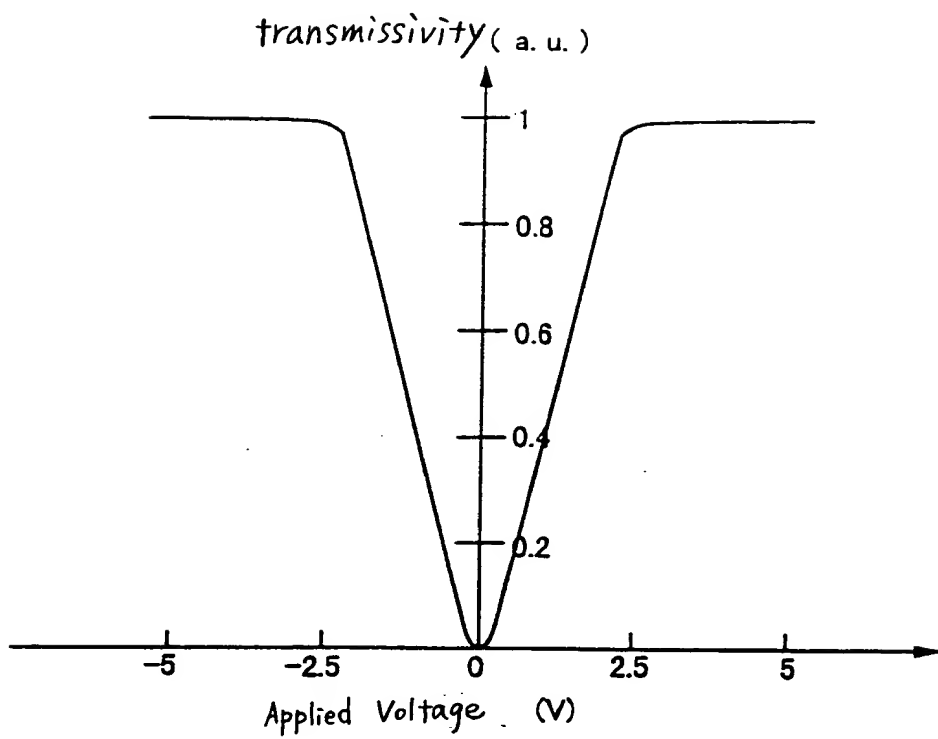


Fig. 31